Amendments to the Specification:

Please add the following heading and paragraph on page 1, after the title and before the first heading:

- Cross-Reference to Related Application

This application is a divisional application of U.S. Patent Application Serial Number 09/952,639 filed on September 13, 2001, which is based on and claims the benefit from prior Japanese Patent Application No. P2000-280829 filed on September 14, 2000, the disclosures of both are incorporated herein by reference. -

Please replace the paragraph beginning on page 16, line 14 with the following paragraph:

The exponential conversion circuit of the present invention is characterized in that the voltage conversion circuits 1A and 1B ~~has~~ have a common-mode detection circuit (CMD) 21 and a common-mode feedback circuit (CFM) 20.

Please replace the paragraph beginning on page 22, line 10 with the following paragraph:

The voltage conversion circuit 1A in a master exponential conversion circuit 6-i (i is 1 through n-1) converts the two reference input voltages Vref1 ~~an~~ and Vref2 to the first and the second differential output voltages on the basis of a gain control signal Vgmcont i. The exponential conversion device 2A creates a first output current which changes exponentially with respect to the first differential output voltage while the exponential conversion device 2B creates the second output current which changes exponentially with respect to the second differential output voltage. Then the current comparison circuit 3 creates the gain control signal Vgmcont i on the basis of the ratio of the first and second output currents.

Please replace the paragraph beginning on page 22, line 22 with the following paragraph:

The output signals Vgmcont1, Vgmcont2, Vgmcont3 . . . ~~Vgmcont (n-1)~~ Vgmcont(n-1) of a plurality of master exponential conversion circuits 6-1, 6-2, 6-3, . . . 6(n-1) are input to a polynomial circuit 7. Furthermore, a plurality (n) of reference input voltages Vref1, Vref2, Vref3 . . . Vrefn and the control input voltage Vc are input to the polynomial circuit 7 and a control input voltage Vc is converted in accordance with a predetermined function.

Please replace the paragraph beginning on page 24, line 25 with the following paragraph:

For example, as shown in FIG. 8, in the case where the current comparison circuit 3 comprises a current mirror circuit in which the area ratio of the MOS transistors M1 and M2 is set to ~~1 : 4~~ 1:4 ("W" in W/L denotes a channel width while "L" denotes a channel length). The ratio of output currents I_{DM1} and I_{DM2} of the two exponential conversion devices becomes ~~1 : 4~~ 1:4.

Please replace the paragraph beginning on page 36, line 7 with the following paragraph:

An output signal of the variable trans-conductance amplifier 307 is input to the gate of the MOS transistor M303. A voltage between the gate and the source of the MOS transistor M303 is Vgs 303. Furthermore, when a current I_{DM3} which flows through the MOS transistor M306 is set to n, the current ~~In (Icont)~~ ln(Icont) which flows through the MOS transistor M307 becomes 1/n with the current mirror circuit.

Please replace the paragraph beginning on page 36, line 15 with the following paragraph:

Then, this exponential conversion output current (gain control signal) ~~In (Icont)~~ ln(Icont) is output from the drain of the MOS transistor M307. Incidentally, ln denotes a logarithm.

Please replace the paragraph beginning on page 36, line 20 with the following paragraph:

Incidentally, an input terminal of the common mode reference voltage Vcom1, an input terminal of the control voltage (control input signal) Vc, a conductance control signal (control voltage which determines the exponential conversion characteristic) Vgmcont, and an output terminal of the exponential conversion output current (gain control signal) ~~In (Icont)~~ ln(Icont) are provided at the slave block 303, respectively.

Please replace the paragraph beginning on page 37, line 1 with the following paragraph:

By the way, in the exponential conversion circuit, limiting a change in the gain with respect to the change in the control signal to a definite scope without being affected by the temperature change can be realized by maintaining the change ratio in the output signal ~~In (Icont)~~ ln(Icont) which linearly changes with respect to the control input signal Vc input to the exponential conversion circuit.

Please replace the paragraph beginning on page 37, line 9 with the following paragraph:

Here, when this exponential conversion characteristic is grasped as a linear function of the exponential conversion output ~~In (Icont)~~ ln(Icont), the exponential conversion circuit realizes primarily the following two circuit operations.

Please replace the paragraph beginning on page 38, line 22 with the following paragraph:

A circuit associated with the feedback loop in the master block 302 realizes an operation of determining a cut piece ~~In (Iref)~~ ln(Iref) of FIG. 12.

Please replace the paragraph beginning on page 41, line 25 with the following paragraph:

The conductances Gm1 and Gm2 are represented in ~~a Expression~~ an expression in ~~t he~~ the following manner.

Please replace the paragraph beginning on page 43, line 23 with the following paragraph:

Here, in the Expression (14), when the logarithm (~~In~~ ln) on both sides are taken, the following relation expression can be obtained.

Please replace the paragraph beginning on page 45, line 12 with the following paragraph:

In this system, in the beginning, the control voltage Vc is input to the gain control circuit (exponential conversion circuit) 11. Furthermore, the gain control signal ~~In, Ve~~ lnVc (or ~~In (Icont)~~ ln(Icont)) is created with the gain control circuit 11. On the other hand, in the variable gain control circuit 10, output signals Outp and Outm are created on the basis of the input signals INp and INm.

Please replace the paragraph beginning on page 45, line 20 with the following paragraph:

Here, since the gain control signal ~~In and Ve~~ lnVc (or ~~In (Icont)~~ ln(Icont)) output from the gain control circuit 11 are input to the variable gain amplifier 10, the gain of the variable gain amplifier 10 changes on the basis of the gain control signal ~~In Ve~~ lnVc (or ~~In (Icont)~~ ln(Icont)). That is, when the bias voltage Vbias which is a gate voltage of the MOS transistors M402 and M403 is changed with the gain control signal ~~In and Ve~~ lnVc (or ~~In (Icont)~~ ln(Icont)), the gain of the variable gain amplifier 10 can be freely changed.

Please replace the paragraph beginning on page 46, line 6 with the following paragraph:

As the gain control circuit 11, the exponential conversion circuit shown in FIG. 11 can be used as it is. In this embodiment, for the sake of simplification of the explanation, the variable gain amplifier 502 is operated in a single input. The variable gain amplifier 502 comprises MOS transistors M503 and M504, resistor devices Rin and RL and a capacitor C. Symbol Vin denotes an input signal of the variable gain amplifier 502, an output signal of the variable gain amplifier, and

the gain of the variable gain amplifier 502 is controlled with the variable gain control signal Ibias (~~In Ve~~ lnVc).

Please replace the paragraph beginning on page 48, line 6 with the following paragraph:

In contrast, in the variable gain amplifier 502 of FIG. 15, the MOS transistors M501 and M502 in the bias circuit 501 and the MOS transistors M503 and M504 in the variable gain amplifier 502 are operated in a weak inversion area, respectively. Furthermore, in the case where the bias current Ibias of the variable gain amplifier 502 is changed by the gain control circuit (exponential conversion circuit) 11 in the scope of one to ten times, the variable gain amplifier 502 can realize a change in the gain of 20 dB portion.

Please replace the paragraph beginning on page 49, line 6 with the following paragraph:

The gain of the former half of the plurality (two in this embodiment) of variable gain amplifiers VGA is controlled with the gain control signal Ibias created with the gain control circuit 11A and the reference block 301A. That is, in a portion surrounded by broken line 601, ~~three~~ these variable gain ~~amplifier VGA is~~ amplifiers VGA are operated in a ~~weak~~ strong inversion area with the gain control circuit 11A and the reference block (bias circuit) 301A.

Please replace the paragraph beginning on page 49, line 14 with the following paragraph:

In contrast, the gain of the latter half of the plurality (three in this embodiment) of variable gain ~~amplifier~~ amplifiers VGA is controlled with the gain control circuit 11B and the gain control bias Ibias (exp.) created with the reference block 301B. That is, in a portion surrounded with the broken line 602, ~~three~~ these variable gain amplifiers ~~VGA's area is~~ VGA are operated in a weak inversion area with the gain control circuit 11B and the reference block (bias circuit) 301B.